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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,226	06/09/2000	David Robert Baldwin	TD-156	3469

7590 11/20/2002

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EXAMINER

TUNG, KEE M

ART UNIT	PAPER NUMBER
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2676

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/591,226

Applicant(s)

BALDWIN, DAVID ROBERT

Examiner

Kee M Tung

Art Unit

2676

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068) in view of Porterfield (6,249,853).

Peddada teaches a graphics processing method (Figs. 4-6) comprising performing 3D graphics rendering in a graphics accelerator subsystem (Fig. 5, 20), using a dedicated graphics memory (22 and 24) as primary memory for rendering accelerator logic; using a system main memory (14) as additional memory to hold textures required by said rendering accelerator logic; and when textures required by said rendering accelerator logic are not present in said dedicated graphics memory, then either downloading said textures from main memory into said graphics memory (Fig. 5, can be download from disk 18 to AGP mem 14 to texture cache 24). However, Peddada fails to explicitly suggest or teach, selectively, when commanded by a software application, allowing said accelerator logic to read textures directly from said main memory without downloading them into said graphics memory. Peddada teaches there are two AGP models. One is known as the AGP DMA model which downloading texture data from main memory into texture cache in the graphics accelerator (col. 1, line 63 through col. 2, line 9) and another is known as AGP Execute model, has 3D

graphics accelerator accessing textures from AGP memory (part of the main memory) via system logic chip over AGP bus (col. 1, lines 50-57). However, Peddada uses a different way to achieve the benefit of AGP Execute model. Porterfield also teaches two AGP models, a DMA and Execute models (col. 6, line 55 through col. 7, line 5). Porterfield teaches an AGP Execute model by add additional mapping mechanism, such as, GART which is also known to Peddada (col. 1, lines 58-62 and col. 9, lines 6-32). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into Peddada in order to use both AGP models and thus to add the flexibility to the system. Therefore, at least claim 1 would have been obvious.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Porterfield (6,249,853) in view of Mergard et al (5,941,968) or Poirion (6,232,990) or Chen et al (6,292,201).

Porterfield teaches a graphics processing chip (Fig. 3, 160) comprising rendering acceleration chip (part of the graphics accelerator 160); and software which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory (MMU portion of the system logic 154, i.e., the same logic for both Fig. 1 and 3, and further see col. 6, lines 22-32 and col. 6, line 55 through col. 8, line 3 and Figs. 4 and 5a). However, Porterfield fails to explicitly suggest or teach the software integrated on the chip with the graphics accelerator chip. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Porterfield into a single chip integrated circuit in order to achieve a low

cost, low space system without sacrificing overall performance. All three of Mergard et al, Poirion or Chen teaches a single chip integrated circuit that combines the graphics accelerator and system logic plus many other system components into a single chip integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Mergard et al, Poirion or Chen into the system of Porterfield in order to provide a single chip integrated circuit as claimed in order to achieve the different advantages as taught by Mergard et al (abstract), Poirion (col. 2, line 4 through col. 3, line 17) or Chen (col. 3, line 35 through col. 4, line 30). Therefore, at least claim 2 would have been obvious.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068) in view of Mergard et al (5,941,968) or Poirion (6,232,990) or Chen et al (6,292,201).

Peddada et al teaches a graphics processing chip (Fig. 5, 20) comprising rendering acceleration chip (part of the graphics accelerator 20); and software which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory (cache management process, col. 4, lines 4-12). However, Peddada et al fails to explicitly suggest or teach the software integrated on the chip with the graphics accelerator chip. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Peddada et al into a single chip integrated circuit in order to achieve a low cost, low space system without sacrificing overall performance. All three of Mergard et al, Poirion or Chen teaches a single chip integrated circuit that combines the graphics accelerator and

Art Unit: 2676

system logic plus many other system components into a single chip integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Mergard et al, Poirion or Chen into the system of Peddada et al in order to provide a single chip integrated circuit as claimed in order to achieve the different advantages as taught by Mergard et al (abstract), Poirion (col. 2, line 4 through col. 3, line 17) or Chen (col. 3, line 35 through col. 4, line 30). Therefore, at least claim 2 would have been obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 703-305-9660. The examiner can normally be reached on Tuesday - Friday from 6:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

kmt
November 18, 2002



Kee M Tung
Primary Examiner
Art Unit 2676